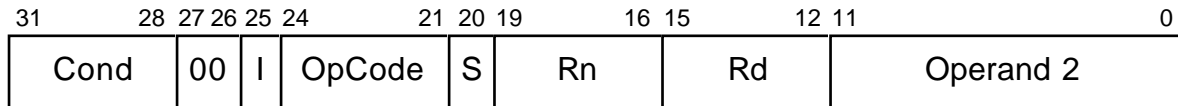


Appendix C



Cond: Condition field

0000	EQ (EQual)
0001	NE (NEver)
0010	CS (Carry Set)
0011	CC (Carry Clear)
0100	MI (MInus)
0101	PL (PLus)
0110	VS (oVerflow Set)
0111	VC (oVerflow Clear)
1000	HI (Hlgher)
1001	LS (Lower or Same)
1010	GE (Greater or Equal)
1011	LT (Less Than)
1100	GT (Greater Than)
1101	LE (Less than or Equal)
1110	AL (ALways)
1111	NV (NeVer)

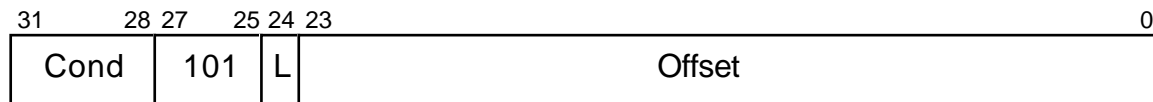
OpCode: Operation code

0000	AND
0001	EOR
0010	SUB
0011	RSB
0100	ADD
0101	ADC
0110	SBC
0111	RSC
1000	TST
1001	TEQ
1010	CMP
1011	CMN
1100	ORR
1101	MOV
1110	BIC
1111	MVN

Instruction set

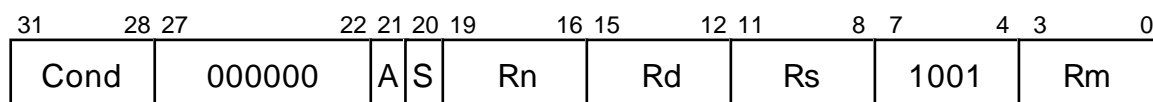
Data Processing

I: Immediate operand bit. This defines exactly what Operand 2 is. If the I bit is 0, Operand 2 is a register, with the register number held in bits 0 to 3 and the shift applied to that register in bits 4 to 11. If the I bit is 1, Operand 2 is an immediate value, with bits 0 to 7 holding the 8 bit value, and bits 8 to 11 holding the shift



applied to that value.

S: Set condition codes. If this bit is set to 0, the condition codes are not altered after the instruction has

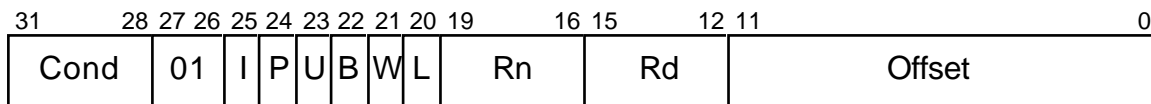


executed. If it is set to 1, they are altered.

Rn: First operand register.

Arm Assembly Language programming

Rd: Destination register.

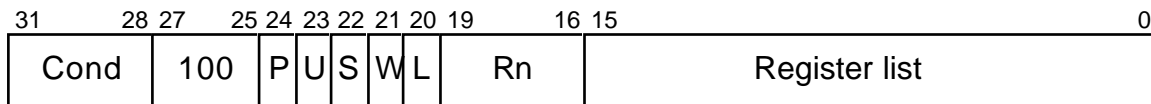


Branch and Branch with link

L: Link bit. 0=Branch, 1=Branch with link

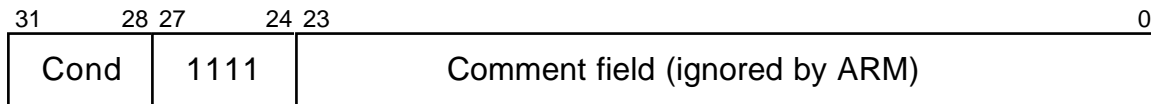
Multiply and multiply-accumulate

A: Accumulate bit. 0=multiply, 1=multiply with accumulate



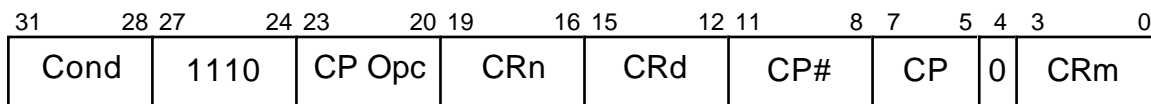
Single Data transfer

P: Pre/Post indexing. 0=post (offset added after transfer). 1=pre (offset added before transfer).



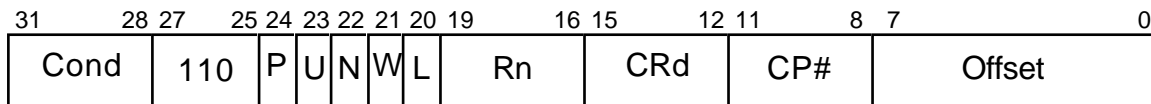
U: Up/Down bit. 0=down (Offset subtracted from base). 1=Up (Offset added to base).

B: Byte/Word bit. 0=transfer word, 1=transfer byte.



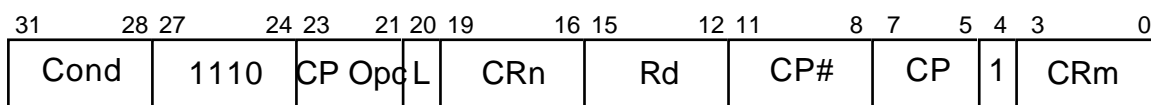
W: Write-back. 0=No write back, 1=Write address into base.

Block data transfer



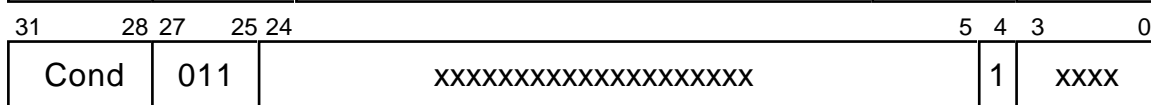
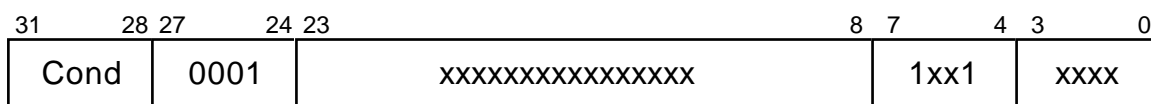
S: PSR & Force user mode. 0=do not load PSR or force user mode. 1=load PSR or force user mode.

Software Interrupt



Co-processor data operations

CP Opc: Co-processor operation code. **CRn:** Co-processor operand register. **CRd:** Co-processor



destination register. **CP#:** Co-processor number. **CP:** Co-processor information

Co-processor data transfers

N: Transfer Length.

Arm Assembly Language programming

Co-processor register transfers

L: Load/Store bit. 0=Store to co-processor, 1=Load from co-processor.

Undefined instructions.